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EXAMINER	
CHOWDHURY, AFROZA Y	
ART UNIT	PAPER NUMBER
2629	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/806,380	RA, DONG-GYUN	
	Examiner	Art Unit	
	AFROZA Y. CHOWDHURY	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 August 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 10-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 10-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/10/2010*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's amendment filed on **August 5, 2010** has been entered. Claims 1-8 and 10-23 are currently pending. Applicant's amended and newly added claims are addressed herein below.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1–8, 12, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Lee et al.** (US Pub. 2002/0057247) in view of **Yu** (US Patent 6,753,855) and in further view of **Nuimura** (US Pub. 2004/0008176).

As to claim 4, Lee et al. discloses a liquid crystal display device, comprising: a liquid crystal module including a liquid crystal panel, a gate driving unit (fig. 3(200)) for delivering scanning signals to the liquid crystal panel, and a data driving unit (fig. 3(300)) for delivering image signals to the liquid crystal panel (fig. 3);

a timing controller (fig. 6(100)) for providing timing signal used to control display of the liquid crystal module ([0099] – [0100], [0121] – [0122]);

a mode setting unit (fig.6(400, 520)) for outputting a control signal according to a selected display mode (page 1, [0020], [0100] – [0102], [0105]);

an inverter control unit (fig. 6(510)) for selectively outputting the timing signal received from the timing controller (fig. 6(100)) according to the control signal from the mode setting unit (fig. 6, [0099] – [0100]);

an inverter (fig. 6(700)) which is operated in synchronous mode when the timing signal is received from the inverter control unit (fig. 6(510, switching unit), [0104] – [0105]); and

a lamp (fig. 6(800)) which is operated by a voltage applied to the lamp according to the operation mode of the inverter (fig. 3, [0098], [0105] – [0107]), wherein

a frequency of the voltage applied to the lamp is synchronized with a frequency of the timing signal during the synchronous mode (fig. 6, [0105] – [0107]).

Lee et al. does not teach an inverter which is operated in an asynchronous mode when the timing signal is not received from the inverter control unit and a frequency of the voltage applied to the lamp is not synchronized with a frequency of the timing signal during the asynchronous mode.

Yu teaches an EL lamp where an inverter which is operated in an asynchronous mode and a frequency of the voltage applied to the lamp is not synchronized with a frequency of the timing signal during the asynchronous mode (col. 1, lines 43-49, col. 2, lines 9-55).

Therefore, it would have been obvious to one skill in the art at the time of the invention was made to incorporate Yu's idea of driving lamp that emits light

asynchronously into the liquid crystal display device (LCD) of Lee et al. to make a LCD device where an inverter operates in synchronous or asynchronous mode with reduced lighting malfunction.

Lee et al. (as modified by Yu) does not explicitly teach an inverter which is operated in both modes synchronous and asynchronous and wherein when the inverter is operated in the synchronous mode, the inverter applies the voltage at a frequency that is synchronized with a frequency of the timing signal, and when the inverter is operated in the asynchronous mode, the inverter applies the voltage at a frequency that is not synchronized with the frequency of the timing signal.

Nuimura teaches an inverter which is operated in both modes synchronous and asynchronous and wherein when the inverter is operated in the synchronous mode, the inverter applies the voltage at a frequency that is synchronized with a frequency of the timing signal, and when the inverter is operated in the asynchronous mode, the inverter applies the voltage at a frequency that is not synchronized with the frequency of the timing signal (figs. 1-6, [0012], [0027], [0029], [0032], [0034] – [0035], [0039]).

Therefore, it would have been obvious to one skill in the art at the time of the invention was made to incorporate Nuimura's idea of using an inverter that operates in both modes synchronous and asynchronous into the liquid crystal display device (LCD) of Lee et al. (as modified by Yu) to make a LCD device where an inverter operates both in synchronous and asynchronous mode where the lamp emits light synchronously and asynchronously according to the mode of operation in order to control brightness with reduced flickering.

Claims 1 and 8 are rejected the same as claim 4 above.

As to claims 2, 5, and 12, Lee et al. teaches a liquid crystal display device wherein the timing signal is a gate select signal or data clock signal (fig. 3, [0093], [0096] – [0097]).

As to claims 3, 6, and 13, Lee et al. discloses a liquid crystal display device wherein the timing signal is a vertical or horizontal synchronous signal (fig. 4, [0104] – [0105]).

As to claim 7, Lee et al. teaches a liquid crystal display device wherein the mode setting unit is included in the timing controller ([0020], [0100] – [0102], [0105]).

6. Claims 10, 11, and 14-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Lee et al.** (US 2002/0057247) in view of **Yu** (US Patent 6,753,855) and **Nuimura** (US Pub. 2004/0008176) and in further view of **Park** (US 20020130830).

As to claim 10, Lee et al. (as modified by Yu and Nuimura) discloses a liquid crystal display device, comprising: a liquid crystal module including a liquid crystal panel, a gate driving unit (fig. 3(200) in Lee et al.) for delivering scanning signals to the

liquid crystal panel, and a data driving unit (fig. 3(300) in Lee et al.) for delivering image signals to the liquid crystal panel (fig. 3 in Lee et al.).

Lee et al. (as modified by Yu and Nuimura) does not explicitly teach a method wherein the steps of outputting a first level control signal when the display mode is the moving-image mode, or outputting a second level control signal when the display mode is the still-image mode.

Park teaches a method wherein the steps of outputting a first level control signal when the display mode is the moving-image mode, or outputting a second level control signal when the display mode is the still-image mode ([0070] – [0071], [0077] – [0078]).

Therefore, it would have been obvious to one skill in the art at the time of the invention was made to include Park's idea of using separate level of control modes into the LCD device of Lee et al. (as modified by Yu and Nuimura) to develop a liquid crystal device with two different level of control modes for moving-image and still-image in order to reduce lighting malfunction.

As to claim 11, Park discloses a method wherein the steps of outputting the timing signal received from the outside when the second level control signal is applied, or not outputting the timing signal received from the outside when the second level control signal is applied ([0077] – [0078], [0080]).

As to claims 14 and 15, Park teaches a liquid crystal display device wherein the display mode is either a moving-image or a still-image mode ([0010]).

As to claim 16, Lee et al. teaches a liquid crystal display device wherein the operation of the lamp is synchronized with the timing signal ([0105]).

Lee et al. does not explicitly teach whether the display mode is the still-image mode when the operation of the lamp is synchronized with the timing signal.

However, it would be obvious for a liquid crystal display device wherein the operation of the lamp is synchronized with the timing signal when the display mode is the still-image mode.

As to claim 17, Lee et al. teaches a liquid crystal display device with an OCD (Optical Compensated Birefringency) mode ([0097]).

Lee et al. does not teach moving image or still image mode.

Park discloses LCD having a driving method of moving picture and still-image mode ([0010] – [0011], [0077] – [0078]).

Therefore, it would be obvious to combine Park's method with the invention of Lee et al. to adapt a method wherein the display mode is either moving-image or still-image mode.

Claims 18-23 are rejected the same as claims 10, 11, and 14-17 above.

Response to Arguments

4. Applicant's arguments filed **August 5, 2010** have been fully considered but they are not persuasive.

On the first page of Remarks, Applicant recited, "**none discloses an inverter that can operate in both synchronous and asynchronous mode**". The examiner respectfully disagrees to this assertion.

Nuimura teaches an inverter which is operated in both modes synchronous and asynchronous and wherein when the inverter is operated in the synchronous mode, the inverter applies the voltage at a frequency that is synchronized with a frequency of the timing signal, and when the inverter is operated in the asynchronous mode, the inverter applies the voltage at a frequency that is not synchronized with the frequency of the timing signal ([0027], [0029], [0032], [0034] – [0035], [0039]).

Park also teaches an inverter (fig. 1(500)) which is operated in both modes synchronous and asynchronous (fig. 8B, [0077] – [0082], Note: backlight luminance processor 282 outputs "first control signal according to the backlight luminance signal" can be considered as "synchronous mode" and "second control signal with no response to the backlight luminance signal" can be considered as "asynchronous mode").

5. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to AFROZA Y. CHOWDHURY whose telephone number is (571)270-1543. The examiner can normally be reached on 7:30-5:00 EST, 5/4/9.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 571-272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AC
10/7/2010

/Bipin Shalwala/
Supervisory Patent Examiner, Art Unit 2629